WHAT IS CLAIMED IS:

1. A method of reducing circuit timing delays, comprising:

selecting a first node;

sorting fan-ins of the first node according to slack values associated with the corresponding fan-ins, wherein at least a portion of the slack values differ in value; and

reducing delays associated with fan-ins having relatively larger negative slack values before reducing delays associated with fan-ins having relatively smaller negative slack values.

2. The method defined in Claim 1, wherein reducing delays is performed recursively.

3. The method defined in Claim 2, wherein recursively reducing delays is performed until the delays cannot be further reduced or timing constraints are violated.

4. The method defined in Claim 1, wherein selecting the first node comprises:

performing a timing analysis on a circuit;

determining a delay target based at least in part on the timing analysis;

determining a slack value for each critical node of the circuit based on the delay target; and

sorting the critical nodes based on the corresponding slack values.

5. The method defined in Claim 4, wherein selecting the first node further comprises selecting a critical node having the largest negative slack.

6. A method of reducing circuit timing delays, comprising:

selecting a first node;

identifying critical fanins of the first node; and

recursively reducing delays associated with at least a portion of the critical fanins of the first node.

7. The method defined in Claim 6, wherein recursively reducing delays is performed on critical fan-ins having relatively larger negative slack values before reducing delays associated with fan-ins having relatively smaller negative slack values.

8. The method defined in Claim 6, additionally comprising performing a local transformation on the first node if the reducing delays for at least one of the critical fanins is not successful.

9. A method of performing circuit delay reduction, comprising:

performing a timing analysis on a circuit;

determining a delay target based at least in part on the timing analysis;

selecting a first output having a negative slack based at least in part on the delay target; and

performing local transformations on transitive fan-ins of the first output to improve the negative slack.

10. The method defined in Claim 9, wherein the first output is a critical output.

11. A method of reducing timing delays for a circuit having primary input (PI) nodes, at least one primary output (PO) node, and a set of circuit nodes between the PI nodes and the PO node(s), the method comprising:

a) identifying a first critical path between a first PI node and a first PO node;

b) beginning at the first PO node, attempting to reduce a delay associated with a first circuit node;

c) determining if the delay reduction meets a first predetermined criteria;

d) identifying a following circuit node in the critical path if the predetermined criteria is not met;

e) attempting to reduce a delay associated with the following circuit node; and

f) repeating c), d) and e) until the delay cannot be reduced or a set of constraints are violated.

12. The method defined in Claim 11, additionally comprising:

g) identifying a second critical path between a second PI node and a second PO node;

h) determining an amount of delay reduction still needed for the second critical path after applying the results of the delay reduction for the first critical path; and

i) beginning at the second PO node, attempting to reduce a delay associated with a second circuit node.

13. The method defined in Claim 11, wherein a critical path is a path that needs to be reduced in delay so as to meet a target timing constraint.

14. The method defined in Claim 11, additionally comprising establishing the criteria.

15. The method defined in Claim 11, wherein the method is performed at a logic optimization phase of a circuit design process.

16. The method defined in Claim 11, wherein the method is performed at a mapping phase of a circuit design process.

17. The method defined in Claim 11, wherein the method is performed at a layout phase of a circuit design process.

18. The method defined in Claim 11, wherein the first PI node and the second PI node are the same.

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19. The method defined in Claim 11, wherein the first PO node and the second PO node are the same.

20. The method defined in Claim 11, wherein a portion of the first critical path overlays a portion of the second critical path.